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EXAMINER	
KARIMY, MOHAMMAD TIMOR	
ART UNIT	PAPER NUMBER
2894	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,001	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	MOHAMMAD Timor KARIMY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 33-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Product-by-Process Limitations

1. While not objectionable, the Office reminds applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, in re *Brown*, 173 USPQ 685; In re Luck, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re* Avery, 186 USPQ 161; *In re* Wethheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Claim Rejections - 35 USC § 102/103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8, 9-10, 16, 18-19 and 33-35 are rejected under 35 U.S.C. 102(b) as anticipated by Ishikawa et al. (US Pub. 2002/0030189 A1) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ishikawa in view of Chen (US Patent 6,211,067 B1).

With respect to claim 1, Ishikawa discloses a thin film transistor comprising:

an insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer fitted in the first opening (note the plug in insulating layer 402 in Fig. 15B);

a second conductive layer on and in contact with the first insulating layer 402 and the first conductive layer (note the conductive impurity regions being in contact with the insulating layer 402 and the plug in Fig. 15B);

wherein the first conductive layer (plug) is thicker than the second conductive layer (impurity regions) in a vertical direction (Fig. 15B), and

wherein a surface of the insulating layer 402 and the first conductive layer (plug) is planarized and uniform surface (see Fig. 15B)

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal or conductive layers in insulating layers). At the time of the invention, it would have

been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

Regarding claim 33, Ishikawa teaches, wherein the insulating layer comprises an inorganic insulating material (e.g. SiOx).

With respect to claim 2, Ishikawa discloses a thin film transistor comprising:

an insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer fitted in the first opening (note the plug in insulating layer 402 in Fig. 15B);

a second conductive layer (impurity or source/drain region) on and in contact with the first insulating layer 402 and the first conductive layer (note the conductive impurity regions being in contact with the insulating layer 402 and the plug in Fig. 15B) ;

wherein the first conductive layer (plug) is thicker than the second conductive layer in a vertical direction (Fig. 15B), and

wherein a surface of the insulating layer 402 and the first conductive layer (plug) is planarized and uniform surface (see Fig. 15B).

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal or conductive layers in insulating layers). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

It is worth mentioning that the limitation "**wherein the second conductive layer is formed by a droplet discharge method using a conductive material**" is a product by process limitation and it does not result to a structurally distinguishable product over the prior art.

With respect to claim 3, Ishikawa discloses a display device comprising:

a first insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer (plug) fitted in the first opening (Fig. 15B);

a second conductive layer (impurity regions) on and in contact with the first insulating layer 402 and the first conductive layer (Fig. 15B);

a semiconductor layer (note the gate electrode, gates are commonly known to be doped polysilicon) over the second conductive layer (impurity regions) with a gate insulating film therebetween (note the unlabelled gate insulating film between gate and impurity regions in Fig. 15B);

a third conductive layer (note the impurity region metal interconnects) over the semiconductor layer (Fig. 15B);

a second insulating layer (note insulating layer having plug 906) having a second opening (opening containing plug 906) over the third conductive layer (see Fig. 15B-16); and

a fourth conductive layer (Conductive plug 906) fitted in the second opening (Fig. 15B or 16);

wherein the first conductive layer (plug) is thicker than the second conductive layer (impurity regions) in a vertical direction (Fig. 15B), and

wherein a surface of the insulating layer 505 and the first conductive layer is planarized and a uniform surface (see Fig. 15B, wherein the insulating layer 402 and the first conductive layer (plug) have a planarized and uniform surface), and

wherein the fourth conductive layer is thicker than the third conductive layer (see Fig. 16).

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does

not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal or conductive layers in insulating layers). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

With respect to claim 4, Ishikawa discloses a display device comprising:

a first insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer (plug) fitted in the first opening (Fig. 15B);

a second conductive layer (impurity regions) on and in contact with the first insulating layer 402 and the first conductive layer (Fig. 15B);

a semiconductor layer (note the gate electrode, gates are commonly known to be doped polysilicon) over the second conductive layer (impurity regions) with a gate insulating film therebetween (note the unlabelled gate insulating film between gate and impurity regions in Fig. 15B);

a third conductive layer (note the impurity region metal interconnects) over the semiconductor layer (Fig. 15B);

a second insulating layer (note insulating layer having plug 906) having a second opening (opening containing plug 906) over the third conductive layer (see Fig. 15B-16); and

a fourth conductive layer (Conductive plug 906) fitted in the second opening (Fig. 15B or 16);

wherein the first conductive layer (plug) is thicker than the second conductive layer (impurity regions) in a vertical direction (Fig. 15B), and

wherein a surface of the insulating layer 505 and the first conductive layer is planarized and a uniform surface (see Fig. 15B, wherein the insulating layer 402 and the first conductive layer (plug) have a planarized and uniform surface), and

wherein the fourth conductive layer 906 is thicker than the third conductive layer (see Fig. 16).

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal or conductive layers in insulating layers). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's

conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

It is worth mentioning that the limitation "**wherein the second conductive layer** by process limitation and it does not result to a structurally distinguishable product over the prior art.

With respect to claim 5, Ishikawa discloses a display device comprising:

a first insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer (plug) fitted in the first opening (Fig. 15B);

a second conductive layer (impurity regions) on and in contact with the first insulating layer 402 and the first conductive layer (Fig. 15B);

a semiconductor layer (note the gate electrode, gates are commonly known to be doped polysilicon) over the second conductive layer (impurity regions) with a gate insulating film therebetween (note the unlabelled gate insulating film between gate and impurity regions in Fig. 15B);

a pair of third conductive layer (note the impurity region metal interconnects 1108) over the semiconductor layer 1104 (Fig. 4A & 15B);

a first electrode 1203 over one of third conductive layers; an electroluminescent layer 1201 over the first electrode 1203; and a second electrode 1200 over the electroluminescent layer 1201 (note that Ishikawa teaches in Fig. 16 wherein the thin film transistors can be combined, overlapped and joined to obtain a semiconductor package. Though the overlapping of Fig. 24A-B is not shown, however, it would have been known to those having ordinary skill in the art to stack the TFT of Fig. 24A-B as described in Fig. 16. In the stacked structure of Fig. 16, the middle TFT structure will have a first electrode 1203 over the source/drain wirings 1108 of the bottom TFT; an electroluminescent layer 1201 over the first electrode 1203 and a second electrode layer 1200 over the El layer 1201 - visualize the stacking of Fig. 24A-B as described in the package showing of Fig. 16).

Ishikawa further teaches wherein the first conductive layer (plug) is thicker than the second conductive layer (impurity regions) in a vertical direction (Fig. 15B), and

wherein a surface of the insulating layer 505 and the first conductive layer is planarized and a uniform surface (see Fig. 15B, wherein the insulating layer 402 and the first conductive layer (plug) have a planarized and uniform surface), and

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal

or conductive layers in insulating layers). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

With respect to claim 6, Ishikawa discloses a display device comprising:

a first insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer (plug) fitted in the first opening (Fig. 15B);

a second conductive layer (impurity regions) on and in contact with the first insulating layer 402 and the first conductive layer (Fig. 15B);

a semiconductor layer (note the gate electrode, gates are commonly known to be doped polysilicon) over the second conductive layer (impurity regions) with a gate insulating film therebetween (note the unlabelled gate insulating film between gate and impurity regions in Fig. 15B);

a pair of third conductive layer (note the impurity region metal interconnects 1108) over the semiconductor layer 1104 (Fig. 4A & 15B);

a first electrode 1203 over one of third conductive layers; an electroluminescent layer 1201 over the first electrode 1203; and a second electrode 1200 over the

electroluminescent layer 1201 (note that Ishikawa teaches in Fig. 16 wherein the thin film transistors can be combined, overlapped and joined to obtain a semiconductor package. Though the overlapping of Fig. 24A-B is not shown, however, it would have been known to those having ordinary skill in the art to stack the TFT of Fig. 24A-B as described in Fig. 16. In the stacked structure of Fig. 16, the middle TFT structure will have a first electrode 1203 over the source/drain wirings 1108 of the bottom TFT; an electroluminescent layer 1201 over the first electrode 1203 and a second electrode layer 1200 over the El layer 1201 - visualize the stacking of Fig. 24A-B as described in the package showing of Fig. 16).

Ishikawa further teaches wherein the first conductive layer (plug) is thicker than the second conductive layer (impurity regions) in a vertical direction (Fig. 15B), and

wherein a surface of the insulating layer 505 and the first conductive layer is planarized and a uniform surface (see Fig. 15B, wherein the insulating layer 402 and the first conductive layer (plug) have a planarized and uniform surface), and

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal or conductive layers in insulating layers). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's

conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

It is worth mentioning that the limitation "**wherein the second conductive layer is formed by a droplet discharge method using a conductive material**" is a product by process limitation and it does not result to a structurally distinguishable product over the prior art.

With respect to claim 7, Ishikawa discloses a display device comprising:

a first insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer (plug) fitted in the first opening (Fig. 15B);

a second conductive layer (impurity regions) on and in contact with the first insulating layer 402 and the first conductive layer (Fig. 15B);

a semiconductor layer (note the gate electrode, gates are commonly known to be doped polysilicon) over the second conductive layer (impurity regions) with a gate insulating film therebetween (note the unlabelled gate insulating film between gate and impurity regions in Fig. 15B);

a pair of third conductive layer (note the impurity region metal interconnects 1108) over the semiconductor layer 1104 (Fig. 4A & 15B);

a first electrode 1203 over one of third conductive layers (Fig. 24B and 16);

a second insulating layer having a second opening over the other one of the pair of third conductive layers (note the insulating layer having the opening housing the plug 906 in Fig. 16);

a fourth conductive layer (plug 906) fitted in the second opening (Fig. 16);

an electroluminescent layer 1201 over the first electrode 1203 (Fig. 24B); and a second electrode 1200 over the electroluminescent layer 1201 (Fig. 24B & 16 - note that Ishikawa teaches in Fig. 16 wherein the thin film transistors can be combined, overlapped and joined to obtain a semiconductor package. Though the overlapping of Fig. 24A-B is not shown, however, it would have been known to those having ordinary skill in the art to stack the TFT of Fig. 24A-B as described in Fig. 16. In the stacked structure of Fig. 16, the middle TFT structure will have a first electrode 1203 over the source/drain wirings 1108 of the bottom TFT; an electroluminescent layer 1201 over the first electrode 1203 and a second electrode layer 1200 over the El layer 1201 - visualize the stacking of Fig. 24A-B as described in the package showing of Fig. 16).

Ishikawa further teaches wherein the first conductive layer (plug) is thicker than the second conductive layer in a vertical direction (Fig. 15B), wherein a surface of the first insulating layer 402 and the first conductive layer (Plug) is planarized and a uniform surface, wherein the fourth conductive layer 906 is thicker than the pair of third conductive layers 1108.

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does

not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal or conductive layers in insulating layers). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

With respect to claim 8, Ishikawa discloses a display device comprising:

a first insulating layer 402 having a first opening (note the unlabelled plug positioned in the opening in insulating layer 402 in Fig. 15B);

a first conductive layer (plug) fitted in the first opening (Fig. 15B);

a second conductive layer (impurity regions) on and in contact with the first insulating layer 402 and the first conductive layer (Fig. 15B);

a semiconductor layer (note the gate electrode, gates are commonly known to be doped polysilicon) over the second conductive layer (impurity regions) with a gate insulating film therebetween (note the unlabelled gate insulating film between gate and impurity regions in Fig. 15B);

a pair of third conductive layer (note the impurity region metal interconnects 1108) over the semiconductor layer 1104 (Fig. 4A & 15B);

a first electrode 1203 over one of third conductive layers (Fig. 24B and 16);

a second insulating layer having a second opening over the other one of the pair of third conductive layers (note the insulating layer having the opening housing the plug 906 in Fig. 16);

a fourth conductive layer (plug 906) fitted in the second opening (Fig. 16);

an electroluminescent layer 1201 over the first electrode 1203 (Fig. 24B); and a second electrode 1200 over the electroluminescent layer 1201 (Fig. 24B & 16 - note that Ishikawa teaches in Fig. 16 wherein the thin film transistors can be combined, overlapped and joined to obtain a semiconductor package. Though the overlapping of Fig. 24A-B is not shown, however, it would have been known to those having ordinary skill in the art to stack the TFT of Fig. 24A-B as described in Fig. 16. In the stacked structure of Fig. 16, the middle TFT structure will have a first electrode 1203 over the source/drain wirings 1108 of the bottom TFT; an electroluminescent layer 1201 over the first electrode 1203 and a second electrode layer 1200 over the El layer 1201 - visualize the stacking of Fig. 24A-B as described in the package showing of Fig. 16).

Ishikawa further teaches wherein the first conductive layer (plug) is thicker than the second conductive layer in a vertical direction (Fig. 15B), wherein a surface of the first insulating layer 402 and the first conductive layer (Plug) is planarized and a uniform surface, wherein the fourth conductive layer 906 is thicker than the pair of third conductive layers 1108 (Fig. 15B & 16).

Though Ishikawa shows planarized and a uniform surface for the conductive layer (plug) and the insulating layer 402; however, if it is determined that Ishikawa does not teach a planarized and uniform surface for the conductive and insulating layers, then Chen patent teaches planarizing the surface of metal plugs and insulating layer by using chemical mechanical polishing (CMP) in order to remove surface roughness and irregularities (Fig. 1A-1E). Ishikawa and Chen are analogous art (both deal with metal or conductive layers in insulating layers). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to planarize the surface of Ishikawa's conductive and insulating layers by CMP process for the benefit of a smooth and uniform surface free of unwanted irregularities. The motivation for planarizing the surfaces by CMP would have been to reduce production cost, shorten production time and consequently increase productivity. Therefore, Ishikawa and Chen would have been combinable.

It is worth mentioning that the limitation "**wherein each of the second conductive layer and the third conductive layer is formed by a droplet discharge method using a conductive material**" is a product by process limitation and it does not result to a structurally distinguishable product over the prior art.

With respect to claim 9, Ishikawa teaches the thin film transistor according to any of claim 1 to 8, wherein the thin film transistor or display device further comprising titanium oxide below the first conductive layer Note the adhesive film in Fig. 14B-C).

With respect to claim 10, Ishikawa teaches the thin film transistor according to any of claims 1 to 8, wherein the thin film transistor or display device further comprises a film comprising aluminum (Para [0305]).

With respect to claim 16, Ishikawa teaches the thin film transistor according to any of claims 3 to 8, wherein the semiconductor layer is a polycrystalline semiconductor (Fig. 15B).

With respect to claims 18, Ishikawa teaches in Fig. 28C the thin film transistor of claims 3 to 8, wherein a television apparatus can include the thin film transistor.

Moreover, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

With respect to claims 19, Ishikawa implicitly teaches in Fig. 9B the thin film transistor of claims 3 to 8, wherein a television apparatus can include the thin film transistor.

Moreover, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Regarding claim 33 and 34, Ishikawa teaches wherein the first insulating layer can comprise an inorganic insulating material (SiOx).

Regarding claim 35, Ishikawa teaches wherein the second insulating layer can comprise an inorganic insulating material (SiOx).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa as applied to claims 1-8 above, and in view of Yamazaki et al. (US Pub. 2002/0132396 A1).

With respect to claims 11-12, Ishikawa does not teach copper as the material used for the second conductive layer; however, the use of copper in conductive wiring is known to those of ordinary skill in the art because of copper's high electrical conductivity. For instance, Yamazaki ('396) discusses the use of copper wiring for electric connection. As such, the use of copper in conductive wiring is within the knowledge of one of ordinary skill in the art.

6. Claims 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa as applied to claims 1 to 8 above.

With respect to claims 13 and 17, Ishikawa does not disclose a range of from 5 to 100 μm for an opening containing the conductive layer or a channel width. Notwithstanding, one of ordinary skill in the art would have been led to the recited

dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

7. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa as applied to claims 1-8 above, and in further view of Young (US Pub. 20010013913 A1).

With respect to claims 14-15, Ishikawa does not teach the use amorphous or semi-amorphous silicon in the semiconductor layer; nonetheless, it is widely known in the semiconductor art to use amorphous semiconductor in TFT active areas. For instance, Young discusses in Fig. 4 amorphous semiconductor gate structures. Therefore, the use of amorphous semiconductor material is TFT active regions would have been obvious to one of ordinary skill in the art.

Response to Arguments

8. Applicant's arguments filed 10/12/2010, have been fully considered but they are moot in view of new grounds of rejection.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad Timor Karimy whose telephone number is 571-272-9006. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mtk

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